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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,068	10/07/2003	Andrew S. Hildebrant	10030549-1	8619

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EXAMINER	
LEIVA, FRANK M	
ART UNIT	PAPER NUMBER
3714	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/681,068	HILDEBRANT ET AL.	
	Examiner	Art Unit	
	FRANK M. LEIVA	3714	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgements

1. The examiner acknowledges claims 3, 7, 8, 13, 14,19 and 20 canceled in the applicant's submission filed 09 August 2007, and new claims 22-25.

Response to Arguments

2. Applicant's arguments filed 06 November 2009 have been fully considered but they are not persuasive for the following reasons:

3. Regarding the argument on page 6 of applicant's remarks; "*With respect to claim 1, the Examiner asserts that Agrawal discloses "determining a required memory needed to execute [a] plurality of test vectors" in col. 4:40-60, where Agrawal discloses a system that determines the minimum required number of flip-flops gates (memory). See, 7/1/2009 Office Action, p. 5. Applicants respectfully disagree.*

Agrawal discloses that:

...A sequential circuit...is fully initialized when all its memory elements are in known states. One has to provide a set of initialization vectors to bring a circuit to a known state, and those initialization vectors must be chosen appropriately. In accordance with our preferred embodiment, the initialization vectors are generated by a procedure that minimizes a "cost function". We chose our cost function to correspond to the number of flip-flops in the "unknown" state, but other cost functions are also possible.

As shown in the flow chart of FIG. 2, the initialization process begins at block 100 with the assumption that all flip-flops are at the "unknown" state, and the cost function is simply equal to the number of flip-flops in the circuit, M. The process of selecting a set of initialization vectors consists of generating "trial vectors" and accepting only those trial vectors that reduce the cost.

Col. 4, lines 43-60.

From the above excerpt, applicants believe it is clear that Agrawal does not disclose an action of "determining a required memory needed to execute [a] plurality of test vectors". Instead, Agrawal discloses an action of determining a number of memory elements (flip-flops) that are affected (or initialized) by one or more initialization vectors".

The examiner considers that the phrase "required memory" is equal to "minimum number of flip-flops" which is obtained by minimizing cost, the cost being "an action of determining a number of flip-flops".

4. Regarding the argument on page **7** of applicant's remarks; "*Given that Agrawal does not disclose "determining a required memory needed to execute the plurality of test vectors", it follows that Agrawal cannot disclose "using the required memory to estimate a cost to execute the test vectors*." Since the argument above is not persuasive, and established that Agrawal does determine the required memory, this argument is moot.

5. Regarding the argument on page 8 of applicant's remarks in reference of the remaining claims 2-5, **7**-16, since the previous arguments are found not persuasive, the remainder of the claims stand rejected as well.

6. The examiner deems applicant's remarks not persuasive and the previous rejection proper.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Agrawal (US 5,257,268).

9. Regarding claims 1, 8 and 13; Agrawal discloses a machine-executable method comprising executing sequences of instructions on a machine, the executed sequences of instructions causing the machine to perform the actions of, (col. 4:33-35), reading a test file having a plurality of test vectors, (col. 3:65-4:1), where the test unit reads previously supplied initialization vectors; determining a required memory needed to execute the plurality of test vectors, (col. 4:40-60), when the system determined the minimum required number of flip-flop gates (memory); and using the required memory to estimate a cost to execute the test vectors, (col. 4:50-52), one of the computed cost functions being equal to the number of required flip-flops (memory).

10. Regarding claims 2 and 14; Agrawal discloses wherein the executed sequences of instructions further cause the machine to perform the action of receiving a billing scheme and wherein using the required memory to estimate a cost includes using the billing scheme to estimate the cost to execute the test vectors,(col. 5:57-61) where the system takes in consideration the budget requirements or "billing scheme".

11. Regarding claims 3, 10 and 15; Agrawal discloses determining a required memory comprises determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board,(col. 6:50-68), multi-level hardware such as multiple boards circuitry is expressed as multiple levels of gate arrays and the cost is estimated by a total of the gates in each level.

12. Regarding claims 4, 11 and 16; Agrawal discloses determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin, (col. 1:16-30).

13. Regarding claims 5 and 12; Agrawal discloses wherein determining a required memory comprises counting the number of test vectors for each of one or more tests in

the test file, (col. 4:49-68), wherein selecting the various trail vectors there is memory allocated to each test vector output.

14. Regarding claim 7; Park discloses wherein the executed sequences of instructions further cause the machine to perform the action of, for each additional test in the test file: for each pin of the tester, determining a third memory requirement for the pin to execute the test vectors for the additional test; and setting the required memory equal to the third memory requirement if the third memory requirement is greater than the required memory, (col. 6:62-68), defining the minimum cost one would has to conclude that it is the largest value of the absolutely required amount.

15. Regarding claim 9: Agrawal discloses wherein the machine further comprises a user interface to display the cost to a user, (col. 5:30-37), where the system has user input devices or GUI to interface with the program by setting parameters such as acceptable cost limits.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 6 and 17 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Agrawal (US 5,257,268).

18. Regarding claims 6 and 17; Agrawal discloses determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file; setting the required memory equal to the first memory requirement; and for each additional pin of the tester, determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement, (col. 6:46-68), wherein the minimum required memory is all summed up depending of the architecture of the CUT (circuit under test), and all the memory required for every pin input and output is totaled. Since all test sequences are done sequentially, it is inherent for the system to generate a signal for every test point input for the duration of the longest sequence or vector. That is if the longest instruction sequence takes 11 clock pulses, then for every input of the CUT there must be 11 sequenced values stepped through with the clock pulses, each value retained in its own memory address.

It should be understood that all limitations of claims 6 and 17 are covered by Agrawal yet in an ambiguous manner and that although inherent in the disclosure it would also surely be obvious to one of ordinary skill in the art to interpret the computing of the test vectors costs for all inputs to mean that each input will analyzed and vectors generated for them, the embodiments as such, infers that all inputs are being tested in that means each and every one input stating with a first input and going down to the last input.

Examiner's Notes

19. Examiner interpretation of a flip-flop gate is one type of memory cell, as depicted on Matsumiya (US 5,367,480), cited here to show interpretation of the state of the art.
20. Examiner has cited paragraphs and figures in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within

the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FRANK M. LEIVA whose telephone number is (571)272-2460. The examiner can normally be reached on M-Th 9:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter D. Vo can be reached on (571) 272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FML
03/11/2010.

/Peter D. Vo/
Supervisory Patent Examiner, Art Unit 3714